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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,906	STEEGEN ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2003 and 28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6-28-04; 8-23-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 05 November 2003 and to applicant's amendment filed on 28 June 2005.

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-23, in the reply filed on 28 June 2005 and cancellation of the non-elected claims 24-36 are acknowledged.

2. Applicant's election with traverse of Species 1, claims 1-18, in the reply filed on 28 June 2005 is acknowledged. The traversal is on the grounds that the search of both species 1 and species 2 should not require a serious burden since they are similar in scope. This is found to be persuasive and the restriction to the patentably distinct species is hereby withdrawn. Accordingly, claims 1-23 will be examined on the merits.

Specification

3. The disclosure is objected to because of the following informalities:

In paragraph [0016], change "p-type" to --n-type-- because Figs. 2(a)-2(j) depict a process for forming n-type devices (see paragraph [0026], first sentence);

In paragraph [0017], change "n-type" to --p-type-- because Figs. 3(a)-3(d) depict a process for forming p-type devices (see paragraph [0041], first sentence);

In paragraph [0038], fourth sentence, change "source/drain regions 30" to --source/drain regions 340 and 341-- because the source/drain regions for the p-type transistors are designated as reference numbers 340 and 341 in Fig. 3(d) (see paragraph [0043], last sentence); and

In paragraph [0044], third sentence, change "gate electrode 242" to --gate electrode 237-- because the gate electrode for the n-type transistors is designated as reference number 237 in Fig. 2(j) (see paragraph [0036], fourth sentence).

Appropriate correction is required.

Claim Objections

4. Claims 11, 18, 23 are objected to because of the following informalities:

In claim 11, line 3, change "doped region" to --doped portion-- for proper antecedence to claim 1, line 3;

In claim 18, line 2, use upper case O to designate oxygen in the chemical abbreviation for silicon oxynitride; and

In claim 23, line 2, use upper case O to designate oxygen in the chemical abbreviation for silicon oxynitride.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7-14, 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "an n-type device" as used in claim 7, line 2 does not particularly point out if it is supposed to be the n-type device from claim 1, lines 1-2 or a different n-type device.

Claim 8 recites the limitation "the deposited patterned photo-resist layer" in lines 1-2. There is insufficient antecedent basis for this limitation in claim 8.

Claims 9-14 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 8.

The term "the strain layer" as used in claim 20, line 1 does not particularly point out if it is supposed to be the strain layer on the semiconductor substrate (claim 19, line 3) or the strain layer in the gap (claim 19, line 8).

The term "the strain layer" as used in claim 21, line 1 does not particularly point out if it is supposed to be the strain layer on the semiconductor substrate (claim 19, line 3) or the strain layer in the gap (claim 19, line 8).

The term "the strain layer" as used in claim 22, line 1 does not particularly point out if it is supposed to be the strain layer on the semiconductor substrate (claim 19, line 3) or the strain layer in the gap (claim 19, line 8).

The term "the step of growing a strain layer" as used in claim 23, lines 1-2 does not particularly point out if it is supposed to be the strain layer on the semiconductor substrate (claim 19, line 3), the strain layer in the gap (claim 19, line 8), or both strain layers.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-2, 7, 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Roberds et al. (US 2002/0086472 A1 – from applicant's IDS filed on 6-28-04).

Referring to Figs. 1-7 and paragraphs [0020] to [0043], Roberds et al. disclose a method for forming MOS transistors that includes the following features:

- A silicon substrate (16) is provided that can be made p-type by doping with boron or n-type by doping with arsenic (see paragraph [0021]);
- Portions of the substrate (16) are removed as shown in Figs. 1-3 to form an opening that tunnels underneath the channel (28) of a transistor (10); and
- A strain layer (34) that can be silicon-germanium is epitaxially grown under the channel as shown in Fig. 4 and as described in paragraphs [0032] to [0034].

These are all of the limitations as set forth in claims 1-2, 7, 17-18 of the applicant's invention.

9. Claims 1, 18-19, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US 6,825,086 B2).

Referring to Figs. 1-4, 9, 11 and column 2, line 46 to column 5, line 50, Lee et al. disclose a method for forming a strained channel CMOS device that includes the following features:

- A silicon wafer (102) is provided that can be doped either n-type or p-type (see column 2, lines 49-51);
- A silicon-germanium epitaxial layer (104) is grown on the wafer (102) as an initially strained layer (see column 2, lines 52-54);

- A silicon layer (108) is grown on the silicon-germanium epitaxial layer (104) (see column 2, lines 58-60);
- A trench (300) is formed by etching through the silicon layer (108) and the silicon-germanium epitaxial layer (104) to the wafer (102) (see column 3, lines 4-5);
- The trench (100) is lined with a silicon oxide liner (400) (see column 3, lines 22-24); and
- NMOS and PMOS transistors are formed on the substrate as shown in Fig. 9 (see column 3, lines 43-48).

These are all of the process limitations as set forth in claims 1, 18-19, 23 of the applicant's invention. Regarding the growing a strain layer in the gap limitation of applicant's independent claims 1, 19, this is a functional limitation that is presumed to be inherent to the above method of Lee et al. because their method is substantially identical to the applicant's method as claimed in claims 1, 18-19, 23. Accordingly, per MPEP section 2112.01, the burden now shifts to the applicant to show that their as claimed method is different.

10. Claims 1, 3-4, 8-12, 15, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (US 6,891,192 B2).

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a

showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Referring to Figs. 3-9 and column 2, line 52 to column 7, line 10, Chen et al. disclose a method for forming PFETs and NFETs that includes the following features:

- A substrate (16) is provided that can include a single crystal region (14) of silicon-germanium (see column 3, line 63 to column 4, line 3);
- The single crystal region (14) can nominally contain as little as 1 % germanium (see column 3, lines 54-62), so it is reasonable to interpret the single crystal region (14) as being silicon that is doped with germanium;
- Trenches (60) are formed in the single crystal region (14) corresponding to source/drain regions of a PFET gate stack (25) as shown in Fig. 5 to form gaps that are not under the PFET channel;
- While the trenches (60) are formed, an NFET gate stack (45) is covered using photoresist as a mask (58), which is subsequently removed (see column 5, lines 57-62 and column 6, lines 9-15);
- A strain layer (62) that is preferably silicon-germanium (see column 3, lines 29-36) is epitaxially grown in the trenches (60) as shown in Figs. 6-7 and as described in column 6, lines 19-41;
- Source/drain regions (66) are grown over the strain layer (62) as shown in Fig. 8 and as described column 6, lines 42-51; and

- Spacers (29, 30) are formed on sidewalls of the PFET gate stack (25) and the NFET gate stack (45) as shown in Figs. 3, 9 and as described in column 5, lines 47-50 and column 6, lines 54-61.

These are all of the limitations as set forth in claims 1, 3-4, 8-12, 15, 18 of the applicant's invention.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 5-6, 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberds et al. (US 2002/0086472 A1 – from applicant's IDS filed on 6-28-04) as applied to claim 1 above, and further in view of Sugawara et al. (US 2001/0003364 A1).

A shown above, Roberds et al. anticipate claim 1 of the applicant's invention. However, Roberds et al. lack the further limitations to claim 1 as set forth in claims 5-6, 8-14 of the applicant's invention. Regarding claims 5-6, 8-10, Sugawara et al. teach the use of resist masks for fabricating NMOS and PMOS transistors on the same silicon substrate and subsequently removing the resist masks (see paragraphs [0023] and [0024]). Regarding claims 11-14, Sugawara et al. teach the formation of shallow trench

isolations (10a) by filling trenches (9) with silicon oxide as shown in Figs. 5A-5C and as described in paragraphs [0040] to [0042].

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Roberds et al. and Sugawara et al. in order to use resist masks for processing NMOS and PMOS devices separately and also for forming isolation trenches, as taught by Sugawara et al. The use of photoresist masks are well known in the semiconductor art as a way to protect regions of a semiconductor substrate while processing exposed regions of the substrate, for example, by using the masks as a pattern to etch the exposed regions as specifically taught by Sugawara et al. (see paragraphs [0023] and [0040]).

13. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6,891,192 B2) as applied to claim 15 above, and further in view of Tweet et al. (US 6,703,293 B2).

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or

(3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As shown above, Chen et al. anticipate claim 15 of the applicant's invention. However, Chen et al. lack the further limitation to claim 15 as set forth in claim 16, which is to use a germanium doping concentration that ranges from 1 x 10^{14} Ge/cm^2 to 1x10^{16} Ge/cm^2. Tweet et al. teach that germanium can be implanted using a dose that ranges from 5 x 10^{13} Ge/cm^2 to 1x10^{15} Ge/cm^2 (see column 4, line 66 to column 5, line 20).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Chen et al. and Tweet et al. in order to dope the substrate of Chen et al. with germanium using ion implantation as taught by Tweet et al. Tweet et al. recognize that ion implantation is one way to dope a semiconductor layer with germanium (see column 4, line 66 to column 5, line 20).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Murakami et al. and Xiang teach field effect transistors that utilize strain layers.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER